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EXAMINER	
RAHMAN, FAHMIDA	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,432	ELBE ET AL.	
	Examiner	Art Unit	
	Fahmida Rahman	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/12/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/16/06* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to communications filed on 4/12/2007.

2. Claims 1, 2, 6, 10, 13, 16, 17 have been amended, claim 18 has been added and no claims have been cancelled. Therefore, claims 1-18 are pending.

Specification

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Applicant's disclosure does not mention the irrational relation required by claim 1, 2, 13. It mentions that arbitrary relation can be adjusted ([0037] of the corresponding PGPUB 2004/0139363). For the rest of the action, it is assumed that irrational ratio is implicit in arbitrary relationship.

Claim Objections

Claim 18 is objected to because of the following informalities: "con-tact" in line 6 needs to be changed to –contact--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "coprocessor" in claim 17 renders the claim indefinite. Claim requires the CPU to be the coprocessor, which is not supported by the definition of coprocessor. A coprocessor is a processor used to supplement the CPU. Therefore, CPU cannot be the coprocessor as required by the claim. For the rest of the action, it is assumed that the CPU is intended to be the cryptographic processor.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Rasmus Nordby (EP 0217486).

For claim 1, Alasti et al teach the following limitations:

An electronic circuit (Fig 1-Fig 5) **comprising:**

- **a CPU** (302) **having a clock connection for receiving a first clock** (CPUCLK of Fig 3) **and a data connection** (lines 55-57 of column 5);
- **a peripheral unit** (DMA interface 206 and DMA devices in Fig 2) **having a clock connection** (DMA_CLK) **and a data connection** (lines 28-39 of column 3 and lines 1-10 of column 4 mention that 102 is a data buffer for the devices, which can be DMA interface or devices connected to DMA interface. As buffers are data buffers, the DMA interface has data connection), **said clock connection being connected to an external clock input** (Fig 4A shows that DMA clock is externally connected) **so that the peripheral unit receives a second clock** (DMA CLK in Fig 3) **which is different from the first clock** (lines 10-15 of column 6 mention that DMA clock is asynchronous to IO gateway clock. The IO gateway clock is in CPU CLK domain shown in Fig 3. Lines 45-51 of column 3 mention that the clock rates are independent) **so that a ratio between a clock frequency of the first clock and a clock frequency of the second clock is irrational** (lines 25-30 of column 7 mention that IO clock ranges from 0 to 50 Mhz, CPU clock ranges from 250 to 300 Mhz. Therefore, suitable choice of DMA and CPU frequencies provides irrational relationship, such as CPU clock 55132783 hz and DMA clock 33333333 Hz);
- **synchronization means** (300; lines 8-10 of column 6) **comprising a first and a second data connection** (lines 59-65 of column 7 mention that data is passed to CPU through 300. Therefore 300 has data connection. The second data

connection is in 300-100 interface and the first data connection is in 300-332 interface), **said first data connection being connected to said data connection of said peripheral unit** (line 60 of column 7);

- **and a data bus** (100) **being connected to said data connection of said central processing unit** (lines 55-57 of column 5) **and to said second data connection of said synchronization means** (Fig 3).

Alasti et al do not explicitly mention the following limitations:

The ratio between first and second clock is irrational, though Alasti's system can be adapted to use irrational relationship.

Applicant's disclosure does not mention the irrational ratio either. It mentions that arbitrary relation can be adjusted ([0037] of the corresponding PGPUB 2004/0139363). Therefore, examiner takes arbitrary relationship a legitimate term for irrational ratio.

Rasmus disclosed a system where a peripheral unit (101) having a clock connection connected to an external clock input (CLKB), so that the peripheral unit receives a second clock which is different from the first clock (CLKB is different from CLKA) and a ratio between a clock frequency of the first clock and a clock frequency of the second clock is irrational (line 24 of page 2 mentions that two clock frequencies have arbitrary relationship, i.e., asynchronous).

Therefore, asynchronous relationship covers the arbitrary relationship.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Alasti and Rasmus. One ordinary skill would be motivated to have an irrational ratio of clock in Alasti, since Alasti allows such clock ratio and that clock ratio provides the flexibility of independence between two units.

For claim 4, the circuit of Fig 3 of Alasti is an integrated circuit.

For claim 13, Alasti et al teach **a method of controlling an electronic circuit** (Fig 1) **having a central processing unit** (302) **and a peripheral unit** (DMA interface 206 and DMA devices in Fig 2) **being connected to each other via a data bus** (100), **comprising:**

- **clocking said CPU by a first clock** (CPU clock of Fig 1);
- **clocking said peripheral unit by a second clock** (DMA CLK in Fig 3) **which is different from the first clock** (lines 10-15 of column 6 mention that DMA clock is asynchronous to IO gateway clock. The IO gateway clock is in CPU CLK domain shown in Fig 3. Lines 45-51 of column 3 mention that the clock rates are independent) **so that a ratio between a clock frequency of the first clock and a clock frequency of the second clock is irrational** (lines 25-30 of column 7 mention that IO clock ranges from 0 to 50 Mhz, CPU clock ranges from 250 to 300 Mhz. Therefore, suitable choice of DMA and CPU frequencies provides

irrational relationship, such as CPU clock 55132783 hz and DMA clock 33333333 Hz);

- **synchronizing data transmitted between said CPU and said peripheral unit via said data bus** (lines 17-19 of column 4).

Alasti et al do not explicitly mention the following limitations:

The ratio between first and second clock is irrational, though Alasti's system can be adapted to use irrational relationship.

Applicant's disclosure does not mention the irrational ratio either. It mentions that arbitrary relation can be adjusted ([0037] of the corresponding PGPUB 2004/0139363). Therefore, examiner takes arbitrary relationship a legitimate term for irrational ratio.

Rasmus disclosed a system where a peripheral unit (101) having a clock connection connected to an external clock input (CLKB), so that the peripheral unit receives a second clock which is different from the first clock (CLKB is different from CLKA) and a ratio between a clock frequency of the first clock and a clock frequency of the second clock is irrational (line 24 of page 2 mentions that two clock frequencies have arbitrary relationship, i.e., asynchronous).

Therefore, asynchronous relationship covers the arbitrary relationship.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Alasti and Rasmus. One ordinary skill would be motivated to have an irrational ratio of clock in Alasti, since Alasti allows such clock ratio and that clock ratio provides the flexibility of independence between two units.

For claim 14, properly chosen frequencies of Alasti are prime with respect to each other irrespective of the unit used to represent the frequencies.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (US Patent 5708801), in view of Alasti et al (US Patent 6263390), further in view of Rasmus Nordby (EP 0217486).

For claim 2, Williams et al teach the following limitations: **The electronic circuit comprising: a processing unit** (13) **having a clock connection for receiving a first clock** (CHIP CLOCK) **and a data connection** (13 receives data from 14, therefore 13 has a data connection); **a peripheral unit** (14) **having a clock connection and a data connection** (Fig 1); **synchronization means comprising a first and a second data connection** (16 takes data from 11 and pass it to 13), **said first data connection being connected to said data connection of said peripheral unit** (the output of 16 is connected to 14 via 13); **and a data bus being connected to said data connection of said processing unit and to said second data connection of said synchronization means** (16 and 13 are connected to each other through two connections. Thus, it comprises a bus), **wherein said processing**

unit (13), **said peripheral unit** (14), **said synchronization means** (16) **and said data bus** (bus between 13 and 16) **are arranged on a common chip** (15 is a chip) **having two external connection devices being arranged to be connectable to two corresponding contact connections of a terminal** (bus 11 and clock generator 12 are connected to the chip), **a first of said external connection devices being connected to said clock connection of said peripheral unit** (11 is connected to the peripheral unit 14 and provide bus clock to 14) **and the second of said external connection devices being connected to said clock connection of said processing unit** (12 is connected to 13 and provide CHIP clock to 13) **so that the peripheral unit receives a second clock which is different from the first clock** (CHIP clock and bus clock are different as explained in lines 50-60 of column 2).

Williams does not teach the following limitations:

so that a ratio between a clock frequency of the first clock and a clock frequency of the second clock is irrational.

Alasti et al teach the following limitations:

CPU receives a first clock (CPU clock of Fig 1);

peripheral unit receives a second clock which is different from the first clock (DMA_CLK) **so that a ratio between a clock frequency of the first clock and a clock frequency of the second clock can be irrational** (lines 25-30 of column 7 mention that IO clock ranges from 0 to 50 Mhz, CPU clock ranges from 250 to 300 Mhz.

Therefore, suitable choice of DMA and CPU frequencies provides irrational relationship, such as CPU clock 55132783 hz and DMA clock 33333333 Hz);

Alasti et al do not explicitly mention the following limitations:
The ratio between first and second clock is irrational, though Alasti's system can be adapted to use irrational relationship.

Applicant's disclosure does not mention the irrational ratio either. It mentions that arbitrary relation can be adjusted ([0037] of the corresponding PGPUB 2004/0139363). Therefore, examiner takes arbitrary relationship a legitimate term for irrational ratio.

Rasmus disclosed a system where a peripheral unit (101) having a clock connection connected to an external clock input (CLKB), so that the peripheral unit receives a second clock which is different from the first clock (CLKB is different from CLKA) and a ratio between a clock frequency of the first clock and a clock frequency of the second clock is irrational (line 24 of page 2 mentions that two clock frequencies have arbitrary relationship, i.e., asynchronous).

Therefore, asynchronous relationship covers the arbitrary relationship.

The combined teachings of Williams, Alasti and Rasmus do not teach the chip card. Examiner takes an official notice that chip laid on a chip card is well known in the art.

It would have been obvious for an ordinary skill in the art at the time the invention was made to combine the teachings of Williams, Alasti and Rasmus. One ordinary skill would be motivated to combine the teachings of Williams, Alasti and Rasmus, as an irrational ratio of clock provides the flexibility of independence between two units. One ordinary skill would be further motivated to include the chip in a card, since placing chip in a card is necessary in designing many systems.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Rasmus Nordby (EP 0217486), further in view of Matsubara (US patent 5569903).

For claim 3, Alasti et al, in view of Rasmus does not teach any common chip card and controllable oscillator.

Matsubara teaches an IC card (Fig 6) with CPU 12, peripheral unit 14, synchronization means 16, data bus (17) and controllable oscillator (15 A is controllable through a trigger signal) where clock connection of peripheral unit is connected to signal output of the controllable oscillator (lines 1-5 of column 8 mention that CLK from oscillator is supplied to other circuits of IC card. Therefore, the peripheral unit receives CLK from oscillator).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have a controllable oscillator providing clock to peripheral device of Alasti et al, since it provides the flexibility to have desired frequency for the peripheral device. Operating bus in one of many frequencies is a desirable feature for power control. In such a case, a controllable oscillator provides the desirable frequency to the user. In addition, one ordinary skill in the art would be motivated at the time the invention was made to have the components in a common chip card, since that is typically done to create a microprocessor based system design. Providing all the components together in a common chip card increases portability and maintenance of a system, since the chip card can be replaced easily in case of failure.

6. Claims 5, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Rasmus, further in view of Heinrich et al (US Patent 6470393).

For claim 5, Alasti et al or Rasmus et al do not teach any controllable oscillator. Heinrich et al teach a system where an electronic circuit comprises a controlling means having a control output that is connected to control input of a controllable oscillator and the control means control the oscillator depending on a control parameter (lines 2-5 of column 4).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have a controllable oscillator with the circuit of Alasti et al, since it provides the flexibility to have desired frequency for the bus. Operating bus in one of many frequencies is a desirable feature for power control. In such a case, a controllable oscillator provides the desirable frequency to the user.

For claim 8, properly chosen frequencies of Alasti do not have common divisor. However, the clock does not come from a controllable oscillator. Heinrich et al teach a controllable oscillator (line 24 of column 4).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have a controllable oscillator within the clock generator of Alasti et al, since controllable oscillator provides the flexibility to have desired frequency for the bus. Operating bus in one of many frequencies is a desirable feature for power control. In such a case, a controllable oscillator provides the desirable frequency to the user.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Rasmus, further in view of Heinrich et al (US Patent 6470393), further in view of Yamamoto (US Patent 5778237).

For claim 6, Alasti, in view of Rasmus, in view of Heinrich does not teach controlling the oscillator depending on energy available. Heinrich controls the oscillator based on characteristics quantities (line 5 of column 4).

Yamamoto et al teach controlling oscillator (Fig 1 shows controlling clock generator. Fig 16 shows clock generator comprises oscillator) depending on energy available for said electronic circuit (Fig 1 shows that clock generator is controlled by 124. The frequency of the circuit depends on the operating mode, i.e., high or low power consumption mode as explained in line 50 of column 5 through line 26 of column 6. Thus, the frequency of the circuit depends on energy available for that particular mode) such that the energy available for said electronic circuit is distributed to the peripheral unit and the CPU (Line 28 of column 9 through line 29 of column 10 mentions about the changing of frequency is different modules. Thus, energy available in low power mode is distributed in CPU and other peripheral module).

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Alasti, Rasmus, Heinrich and Yamamoto. One ordinary skill in the art would be motivated to control oscillator depending on energy available, since power controlling operation typically adjusts frequency based on power available, which typically comprises controlling oscillator. The controlled frequency ensures low power mode where available energy is distributed to the peripheral unit and CPU.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Rasmus, in view of Heinrich et al (US Patent 6470393), further in view of Yamaguchi (EP 0569131).

For claim 7, properly chosen frequencies of Alasti do not have common divisor. However, the clock does not come from a controllable oscillator. Heinrich et al teach a controllable oscillator (line 24 of column 4).

It would have been obvious for an ordinary skill in the art at the time the invention was made to have a controllable oscillator within the clock generator of Alasti et al, since controllable oscillator provides the flexibility to have desired frequency for the bus. Operating bus in one of many frequencies is a desirable feature for power control. In such a case, a controllable oscillator provides the desirable frequency to the user.

The combination of Alasti, Rasmus and Heinrich et al do not teach that peripheral clock connection has more frequency than CPU frequency. Yamaguchi teaches a circuit where peripheral device has higher frequency than CPU (Fig 4). It would have been obvious for an Ordinary skill in the art to have the peripheral connection with higher clock frequency than CPU clock frequency, since some peripheral device can run faster than CPU.

9. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Rasmus Nordby (EP 0217486), in view of Applicant's Admission of Prior Art.

For claim 9, Alasti et al or Rasmus do not teach cryptographic controller. Applicant admits that conventional circuitry of Fig 6 is a cryptography controller.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Alasti et al and Applicant's Admission of Prior Art. One ordinary skill in the art would have been motivated to have the cryptography controller, since cryptography is very useful tool for ensuring security.

For claim 10, AAPA shows 920a and 920b as coprocessors. Since, Fig 6 is a cryptography controller, it must process some cryptographic algorithm.

For claim 11, Fig 6 of AAPA comprises two coprocessors. However, AAPA does not mention that the peripheral unit being connected to oscillator.

Examiner takes an official notice that coprocessor connected to controllable oscillator is well known in the art. One ordinary skill in the art would have been motivated to connect controllable oscillator to coprocessor, since controllable oscillator produce clock to operate the coprocessors.

For claim 12, the two coprocessors operate in parallel performing various tasks as mentioned in [0012] of AAPA. Since Fig 6 shows the cryptography controller, the tasks should be encrypting/decrypting.

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Voit (US Patent 6510473), further in view of Lloyd et al (US Patent 6175280).

For claim 15, Alasti et al teach the following limitations:

An electronic circuit (Fig 1-Fig 5) **comprising:**

- **a CPU** (302) **having a clock connection for receiving a first clock** (CPUCLK of Fig 3) **and a data connection** (lines 55-57 of column 5);
- **a peripheral unit** (104-108) **having a clock connection** (PCI_CLK) **and a data connection** (lines 20-25 of column 4), **so that the peripheral unit receives a second clock** (PCI CLK in Fig 3) **which is different from the first clock** (lines 9-12 of column 2) **and whose frequency is relatively prime with respect to the first clock** (lines 25-30 of column 7 mention that PCI clock ranges from 0 to 66 Mhz, CPU clock ranges from 250 to 300 Mhz. Therefore, suitable choice of PCI and CPU frequencies provides prime relationship, such as CPU clock 200 Mhz and PCI clock 43111 Hz);

- **synchronization means** (102) **comprising a first and a second data connection** (210, 110), **said first data connection being connected to said data connection of said peripheral unit** (210 is connected to PCI device);
- **and a data bus** (100) **being connected to said data connection of said central processing unit** (lines 55-57 of column 5) **and to said second data connection of said synchronization means** (Fig 1).

Alasti et al do not explicitly mention the following limitations:

Clock connection of peripheral unit is connected to a signal output of a controllable oscillator. However, Fig 3 shows that PCI CLK is inputted into PCI host 324. Therefore, PCI CLK is an external clock input to the peripheral device.

Voit teaches a system where peripheral PCI device receives CLK input from PLL (Fig 2; lines 54-55 of column 4). PLL typically uses voltage controlled oscillator to produce the output clock signal (lines 5-20 of column 5 of Lloyd et al). Therefore, peripheral device connected to controllable oscillator is well known in the art.

It would have been obvious for an ordinary skill in the art at the time the invention was made to combine the teachings of Alasti et al, Voit and Lloyd et al. One ordinary skill would be motivated to have the clock of peripheral PCI device from a signal output of the controllable oscillator (i.e., PLL) as that is the conventional way of providing clock in PCI bus. PLL provides stable frequency synthesis and fast settling times. Therefore,

using PLL with VCO to provide clock in peripheral PCI device has many benefits, such as constant phase and frequency relationship between input and output signal.

11. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Collins et al (US Patent 6378072), further in view of Yamamoto (US patent 5778237).

For claim 16, Alasti et al teach the following limitations:

An electronic circuit (Fig 1-Fig 5) **comprising:**

- **a CPU** (302) **having a clock connection for receiving a first clock** (CPUCLK of Fig 3) **and a data connection** (lines 55-57 of column 5);
- **a peripheral unit** (104-108) **having a clock connection** (PCI_CLK) **and a data connection** (lines 20-25 of column 4), **so that the peripheral unit receives a second clock** (PCI CLK in Fig 3) **which is different from the first clock** (lines 9-12 of column 2) **and whose frequency is independent from the first clock** (lines 49-51 of column 3);
  - **synchronization means** (102) **comprising a first and a second data connection** (210, 110), **said first data connection being connected to said data connection of said peripheral unit** (210 is connected to PCI device);
  - **and a data bus** (100) **being connected to said data connection of said central processing unit** (lines 55-57 of column 5) **and to said second data connection of said synchronization means** (Fig 1).

Alasti et al do not explicitly mention the following limitations:

Clock connection of peripheral unit is connected to a signal output of a controllable oscillator and the peripheral unit is a cryptographic processor. Collins et al disclose a CPU as a cryptographic processor (Fig 1).

It would have been obvious for an ordinary skill in the art at the time the invention was made to combine the teachings of Alasti et al and Collins et al. One ordinary skill in the art would be motivated to design the I/O devices of Alasti et al as a cryptographic processor, since cryptographic operation provides the necessary security in a system. The CPU clock frequency of Alasti et al ranges from 250 Mhz to 300Mhz, which is able to perform cryptographic computation. When performing cryptographic computation, the I/O devices can include cryptographic processor.

Alasti, in view of Collins does not teach any controllable oscillator.

Yamamoto et al teach controlling oscillator (Fig 1 shows controlling clock generator. Fig 16 shows clock generator comprises oscillator) depending on energy available for said electronic circuit (Fig 1 shows that clock generator is controlled by 124. The frequency of the circuit depends on the operating mode, i.e., high or low power consumption mode as explained in line 50 of column 5 through line 26 of column 6. Thus, the frequency of the circuit depends on energy available for that particular mode) such that the energy available for said electronic circuit is distributed to the peripheral unit and the CPU (Line

28 of column 9 through line 29 of column 10 mentions about the changing of frequency is different modules. Thus, energy available in low power mode is distributed in CPU and other peripheral module) and the computing speed with the energy available for said electronic circuit is optimized (as the V-f combination is determined by the available power, it is possible to operate the circuitry with maximized frequency with corresponding voltage. Lines 12-32 of column 18 mention that frequency can be increased. For a low power mode, the maximum frequency can be selected).

Although, Yamamoto does not directly mention about maximizing speed, V-f combination is determined by the available power, therefore, it is possible to operate the circuitry with maximized frequency.

It would have been obvious for one ordinary skill in the art at the time the invention was made to combine the teachings of Alasti, Collins and Yamamoto. One ordinary skill in the art would be motivated to control oscillator depending on energy available, since power controlling operation typically adjusts frequency based on power available, which typically comprises controlling oscillator. The controlled frequency ensures low power mode where available energy is distributed to the peripheral unit and CPU.

12. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Alasti et al (US Patent 6263390), in view of Collins et al (US Patent 6378072).

For claim 17, Alasti et al teach the following limitations:

A method of controlling an electronic circuit (Fig 1) **having a central processing unit** (302) **and a peripheral unit** (DMA interface 206 and DMA devices in Fig 2) **being connected to each other via a data bus** (100), **comprising:**

- **clocking said CPU by a first clock** (CPU clock of Fig 1);
- **clocking said peripheral unit by a second clock which is different from the first clock** (DMA_CLK), **so that the clock frequency of the second clock is independent from the clock frequency of the first clock** (lines 10-15 of column 6 mention that DMA clock is asynchronous to IO gateway clock. The IO gateway clock is in CPU CLK domain shown in Fig 3. Lines 45-51 of column 3 mention that the clock rates are independent); and
- **synchronizing data transmitted between said central processing unit and said peripheral unit via said bus** (lines 17-19 of column 4).

Alasti et al do not teach that the CPU is a cryptographic processor. Collins et al disclose a CPU as a cryptographic processor (Fig 1).

It would have been obvious for an ordinary skill in the art at the time the invention was made to combine the teachings of Alasti et al and Collins et al. One ordinary skill in the art would be motivated to design the CPU of Alasti et al as a cryptographic processor, since cryptographic operation provides the necessary security in a system. The CPU clock frequency of Alasti et al ranges from 250 Mhz to 300Mhz, which is able to perform

cryptographic computation. When performing cryptographic computation, the CPU of Alasti et al can be considered as cryptographic processor.

Allowable Subject Matter

Claim 18 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection. As Alasti is still relied upon for rejection, Examiner is addressing arguments regarding Alasti.

Applicant argues that nothing in Alasti suggests using asynchronous clock in connection with devices other than I/O devices. Therefore, Alasti's teaching should not be transferred to other peripherals.

Examiner disagrees. The I/O devices in Alasti can be a cryptographic co-processor. Lines 50-55 of column 3 of Collins mention that 100 is connected to PCI bus. In other words, it is a PCI I/O device. Therefore, the asynchronous relationship is applicable to cryptographic co-processor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fahmida Rahman whose telephone number is 571-272-8159. The examiner can normally be reached on Monday through Friday 8:30 - 5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fahmida Rahman
Examiner
Art Unit 2116